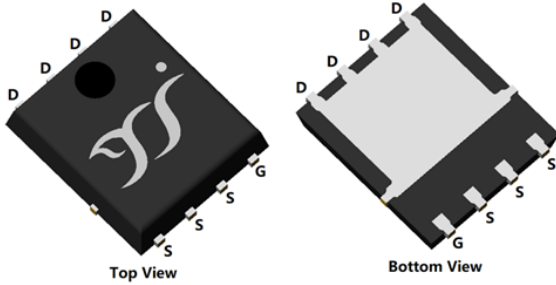
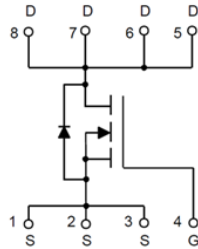


## N-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L



### Product Summary

- $V_{DS}$  80V
- $I_D$  100A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <4.5mohm
- 100% EAS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

### Applications

- Battery protection
- Load switch
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	80	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ C$	$I_D$	100	A
	$T_C=100^\circ C$		63	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	400	A
Avalanche energy <sup>B</sup>		EAS	600	mJ
Total Power Dissipation <sup>C</sup>	$T_C=25^\circ C$	$P_D$	152	W
	$T_C=100^\circ C$		61	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Thermal resistance

Parameter		Symbol	Limit	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	$t \leq 10S$	$R_{\theta JA}$	22.3	$^\circ C/W$
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State		40.7	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.819	

### ■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG100G08A	F1	YJG100G08A	5000	10000	100000	13" reel



# YJG100G08A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	80	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	3.6	4.5	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V	-	0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	100	A
Gate resistance	R <sub>G</sub>	f=1MHz	-	2	-	Ω
Transconductance	G <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =50A		71.5		S
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, f=1MHZ	-	5666	-	pF
Output Capacitance	C <sub>oss</sub>		-	860	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	7.5	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =40V , V <sub>GS</sub> =10V , I <sub>D</sub> =50A	-	73	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	25	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	12	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =50A , di/dt=100A/us	-	50	-	
Reverse Recovery Time	t <sub>rr</sub>		-	44	-	
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DS</sub> =40V , V <sub>GS</sub> =10V , R <sub>G</sub> =3Ω, I <sub>D</sub> =50A	-	27	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	32	-	
Turn-off Delay Time	t <sub>d(off)</sub>		-	54	-	
Turn-off fall Time	t <sub>f</sub>		-	17	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T<sub>J</sub>=25°C, V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=3mH I<sub>as</sub>=20A.

C. P<sub>d</sub> is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R<sub>θJA</sub> is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> =25° C.



■ Typical Performance Characteristics

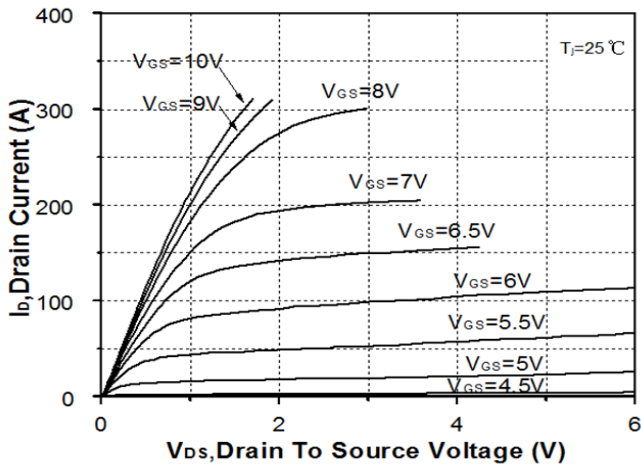


Figure1. Output Characteristics

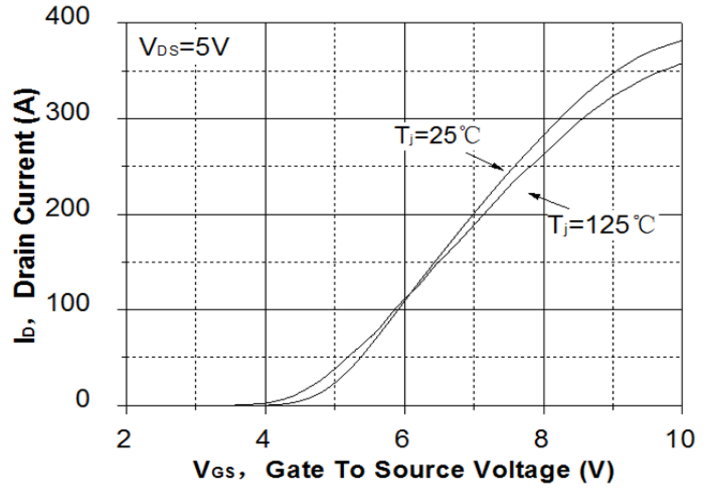


Figure2. Transfer Characteristics

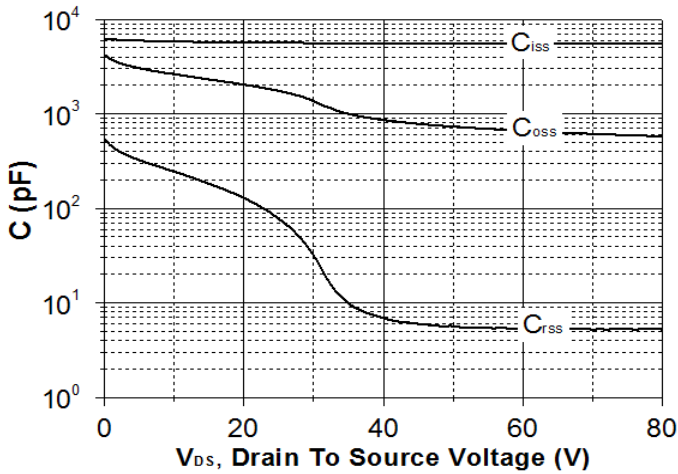


Figure3. Capacitance Characteristics

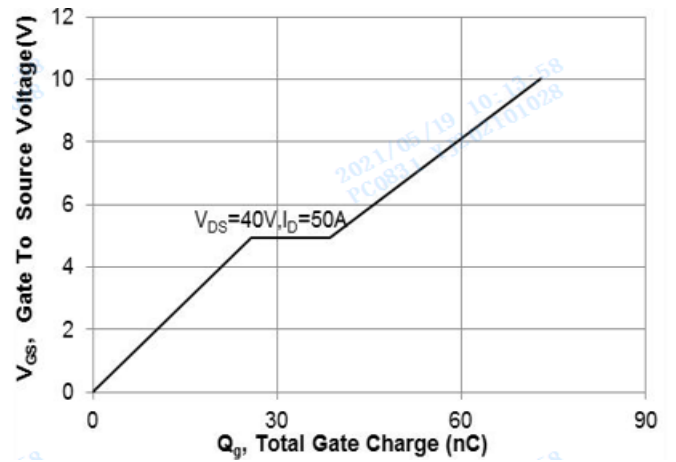


Figure4. Gate Charge

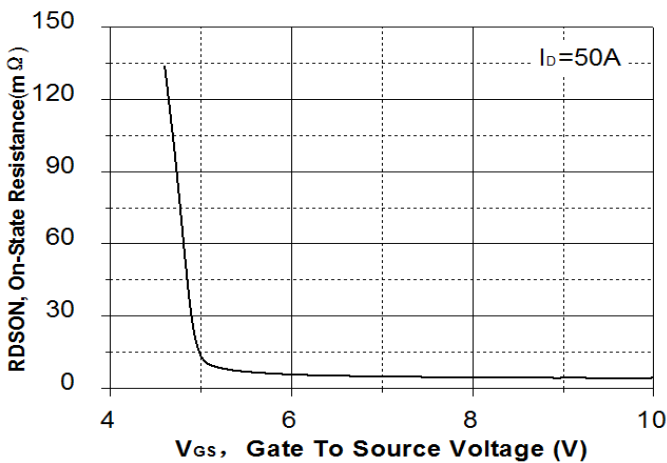


Figure5. On-Resistance vs. Gate to Source Voltage

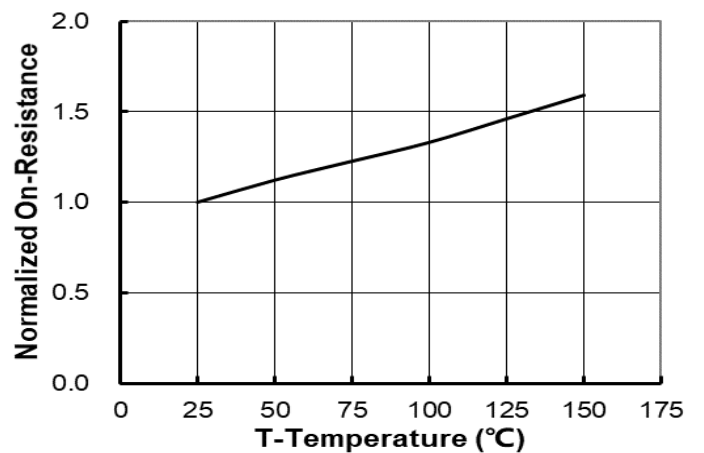


Figure6. Normalized On-Resistance



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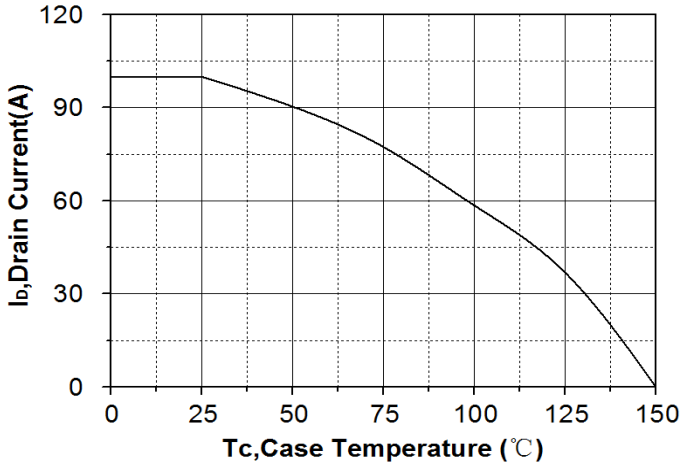


Figure7. Drain current

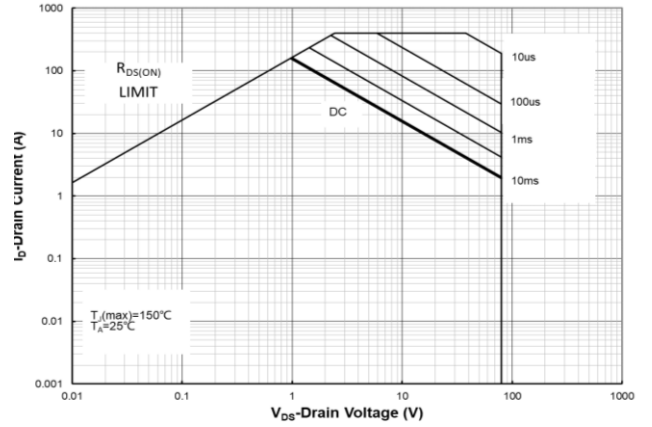


Figure8. Safe Operation Area

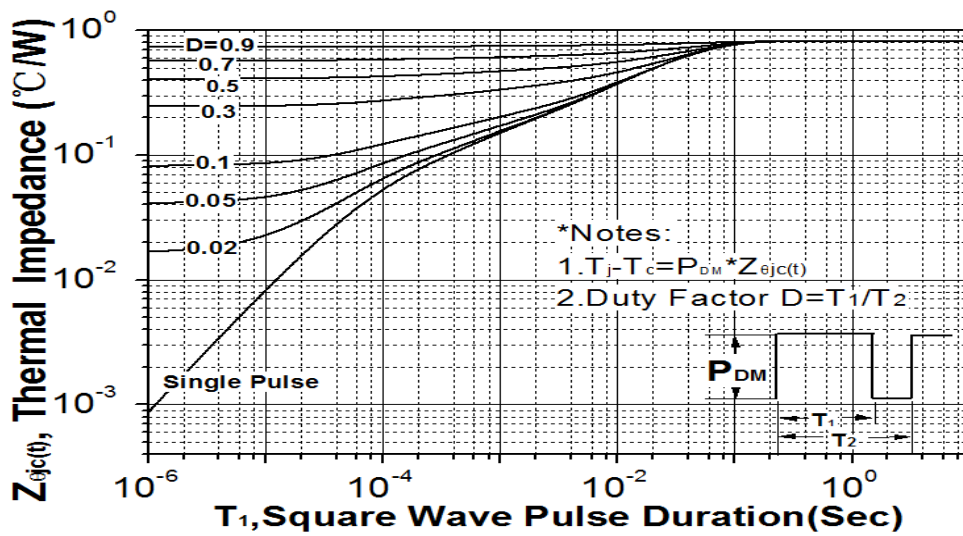
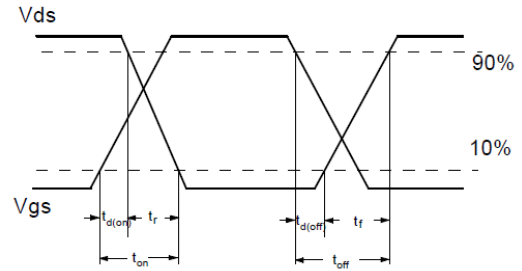
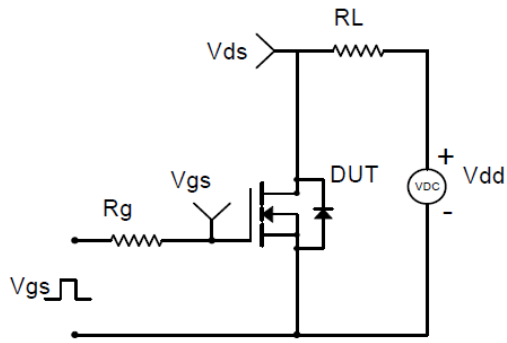
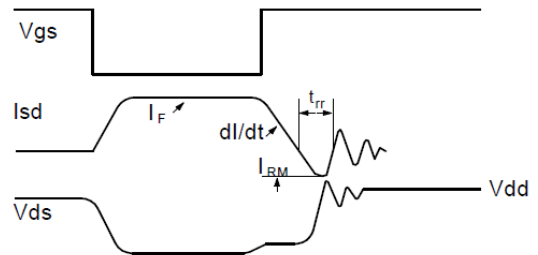
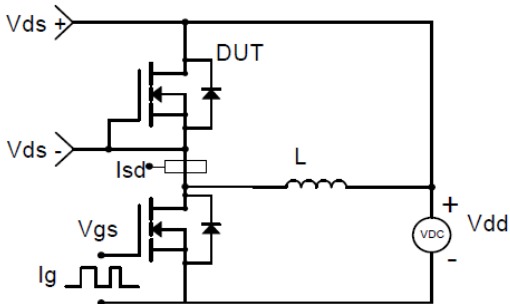


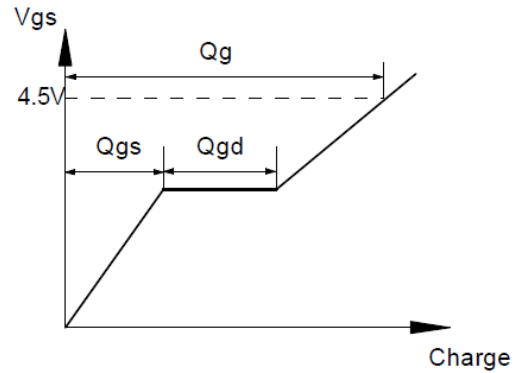
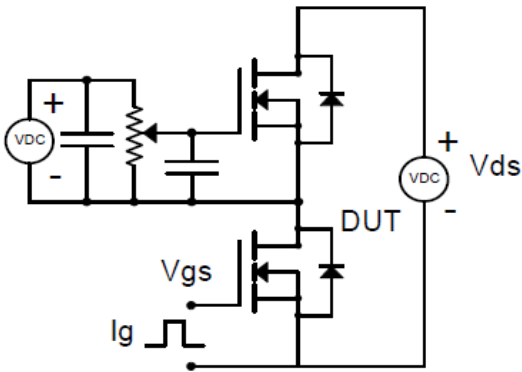
Figure9. Normalized Maximum Transient thermal impedance



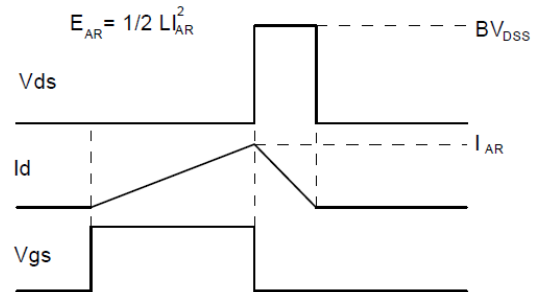
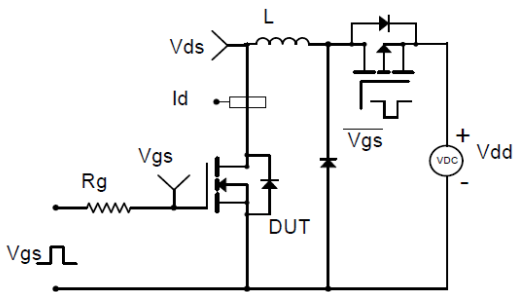
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

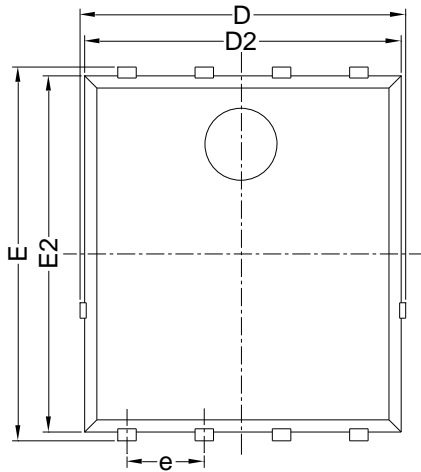


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

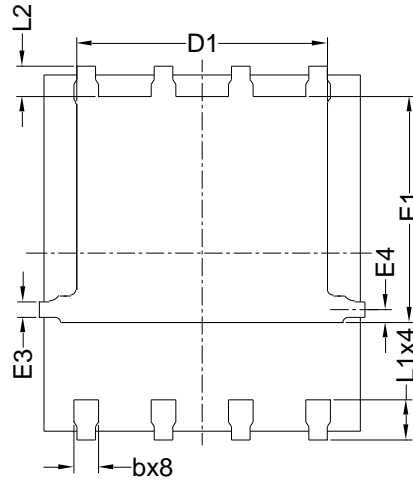


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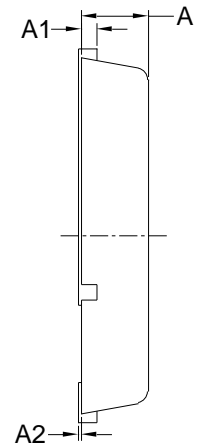
## ■ PDFN5060-8L-B-1.1MM Package information



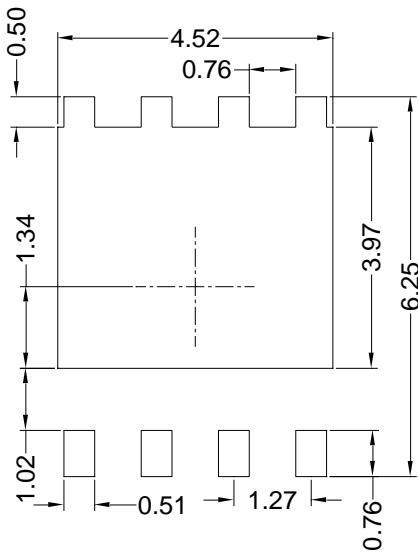
Top View  
正面视图



Bottom View  
背面视图



Side View  
侧面视图



Suggested Solder Pad Layout  
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254 REF		
E4	0.21 REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10$ mm.
3. The pad layout is for reference purposes only.



## YJG100G08A

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